USB2833
User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

In the fields of Real-time Signal Processing, Digital Image Processing and others, high-speed and high-precision data acquisition modules are demanded. ART USB2833 data acquisition module, which brings in advantages of similar products that produced in china and other countries, is convenient for use, high cost and stable performance.

ART USB2833 is a data acquisition module based on USB bus. It can be directly inserted into USB interface to constitute the laboratory, product quality testing center and systems for different areas of data acquisition, waveform analysis and processing. It may also constitute the monitoring system for industrial production process.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- USB2833 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

Analog Input

- Converter Type: AD7321
- Input Range: ±10V, ±5V (default), ±2.5V, 0～10V
- 12-bit resolution
- AD Chip Frequency Conversion: maximum 500KS/s
- Analog Input Mode: 16SE/8DI
- Programmable Gain: 1, 2, 4, 8 (AD8251 default)or 1, 2, 5, 10 (AD8250) or 1, 10, 100, 1000 (AD8253)
- Analog Input Resistance: 10MΩ
- AD Conversion Time: ≤1.6us
- Non-linear error: ±1LSB (Maximum)
- System Measurement Accuracy: 0.1%
- Operating Temperature Range: 0℃~55℃
- Storage Temperature Range: -20℃~70℃

Analog Output

- Converter Type: AD5724
- Output Range: ±10.8V, ±10V, ±5V, 0~10.8V,0~10V, 0~5V
- 12-bit resolution
- Set-up Time: 10μs

- Channel No.: 4-channel
- Non-linear Error: ±1LSB(Max)
- Output Error (full-scale): ±1LSB
- Operating Temperature Range: 0℃~55℃
- Storage Temperature Range: -20℃~5+70℃

Digital Input

- Channel No.: 8-channel
- Electric Standard: TTL compatible
- High Voltage: ≧2.0V
- Low Voltage: ≦0.8V

Digital Output

- Channel No.: 8-channel
- Electrical Standard: TTL compatible
- High Voltage: ≧4.45V
- Low Voltage: ≦0.5V
- Power on reset

Counter

- 16-bit resolution
- Channel No.: 3-channel subtracting counters
- Counting Mode: 6 counting mode (software-configurable)
- Electrical Standard: TTL level
- Clock Source (CLKn): 1Hz~10MHz
- Gate (GATEn): Rising, high-level and low-level
- Counter Output (OUTn): high-level, low-level

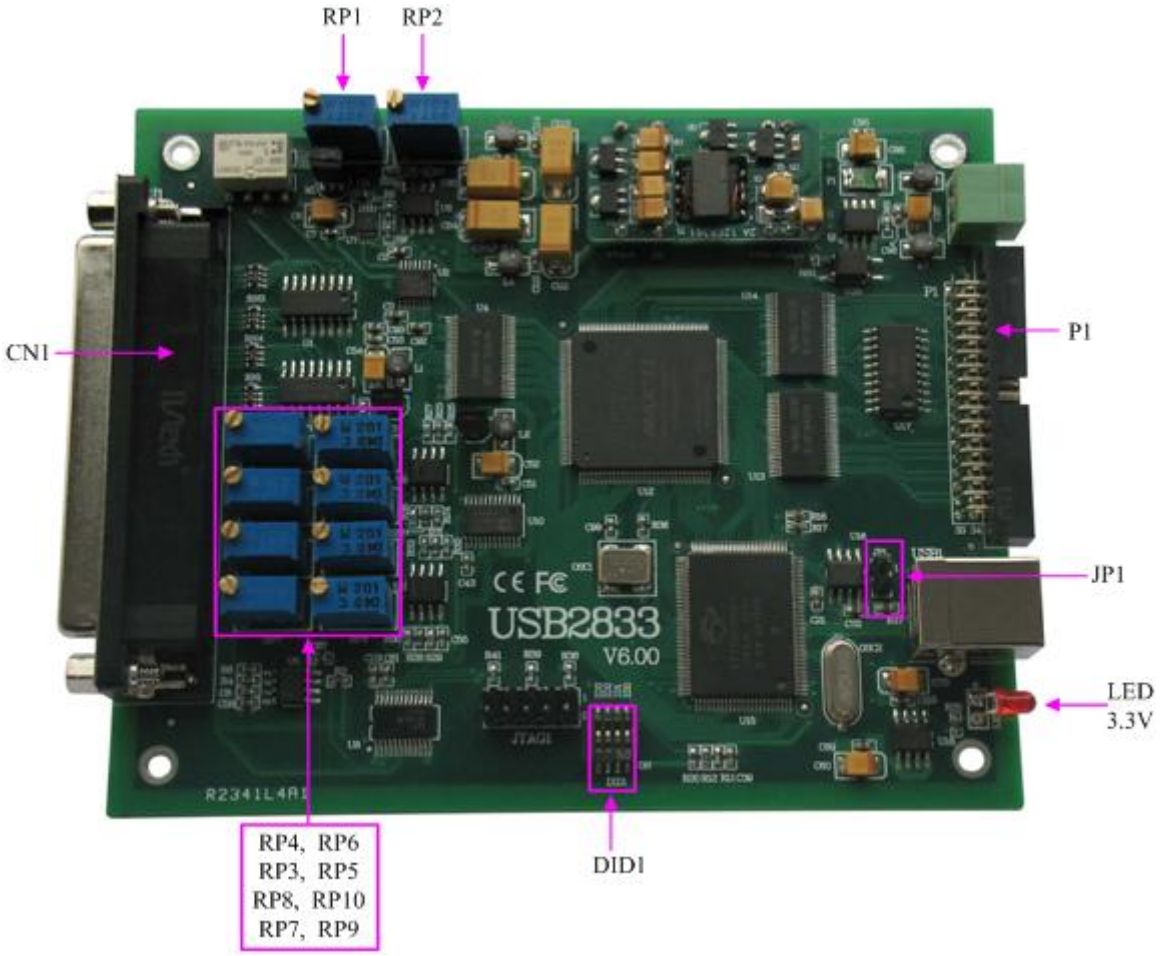
Other Features

Board Clock Oscillation: 40MHz

Dimension: 120mm (L) * 98.5mm (W) * 16mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram



2.2 The Function Description for the Main Component

2.2.1 Signal Input and Output Connectors

CN1: analog signal input/output connector
P1: digital and counter signal input/output connector

2.2.2 Potentiometer

RP1: Analog signal input full-scale adjustment potentiometer
RP2: Analog signal input zero-point adjustment potentiometer
RP4: Analog signal output AO0 zero-point adjustment potentiometer

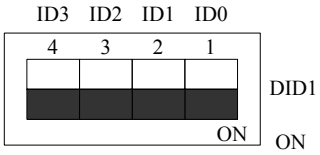
RP8: Analog signal output AO1 zero-point adjustment potentiometer
RP3: Analog signal output AO2 zero-point adjustment potentiometer
RP7: Analog signal output AO3 zero-point adjustment potentiometer
RP6: Analog signal output AO0 full-scale adjustment potentiometer
RP10: Analog signal output AO1 full-scale adjustment potentiometer
RP5: Analog signal output AO2 full-scale adjustment potentiometer
RP9: Analog signal output AO3 full-scale adjustment potentiometer

2.2.3 Jumper

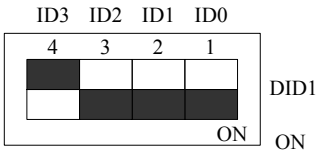
JPW1: load USB controller program, 1-2 shorted (default)

2.2.4 Physical ID of DIP Switch

DID1: Set physical ID number. When the PC is installed more than one USB2833 , you can use the DIP switch to set a physical ID number for each board, which makes it very convenient for users to distinguish and visit each board in the progress of the hardware configuration and software programming. The following four-byte numbers are expressed by the binary system: When DIP switch points to "ON", that means "1", and when it points to the other side, that means "0." As they are shown in the following diagrams: byte "ID3" is the high byte."ID0" is the low byte, and the black part in the diagram represents the location of the switch. (Test software of the company often uses the logic ID management equipments and at this moment the physical ID DIP switch is invalid. If you want to use more than one kind of the equipments in one and the same system at the same time, please use the physical ID as much as possible.).



The above chart shows"1111", so it means that the physical ID is 15.



The above chart shows"0111", so it means that the physical ID is 7.

The above chart shows"0101", so it means that the physical ID is 5.

ID3	ID2	ID1	ID0	Physical ID（Hex）	Physical ID（Dec）
OFF（0）	OFF（0）	OFF（0）	OFF（0）	0	0
OFF（0）	OFF（0）	OFF（0）	ON（1）	1	1

OFF（0）	OFF（0）	ON（1）	OFF（0）	2	2
OFF（0）	OFF（0）	ON（1）	ON（1）	3	3
OFF（0）	ON（1）	OFF（0）	OFF（0）	4	4
OFF（0）	ON（1）	OFF（0）	ON（1）	5	5
OFF（0）	ON（1）	ON（1）	OFF（0）	6	6
OFF（0）	ON（1）	ON（1）	ON（1）	7	7
ON（1）	OFF（0）	OFF（0）	OFF（0）	8	8
ON（1）	OFF（0）	OFF（0）	ON（1）	9	9
ON（1）	OFF（0）	ON（1）	OFF（0）	A	10
ON（1）	OFF（0）	ON（1）	ON（1）	B	11
ON（1）	ON（1）	OFF（0）	OFF（0）	C	12
ON（1）	ON（1）	OFF（0）	ON（1）	D	13
ON（1）	ON（1）	ON（1）	OFF（0）	E	14
ON（1）	ON（1）	ON（1）	ON（1）	F	15

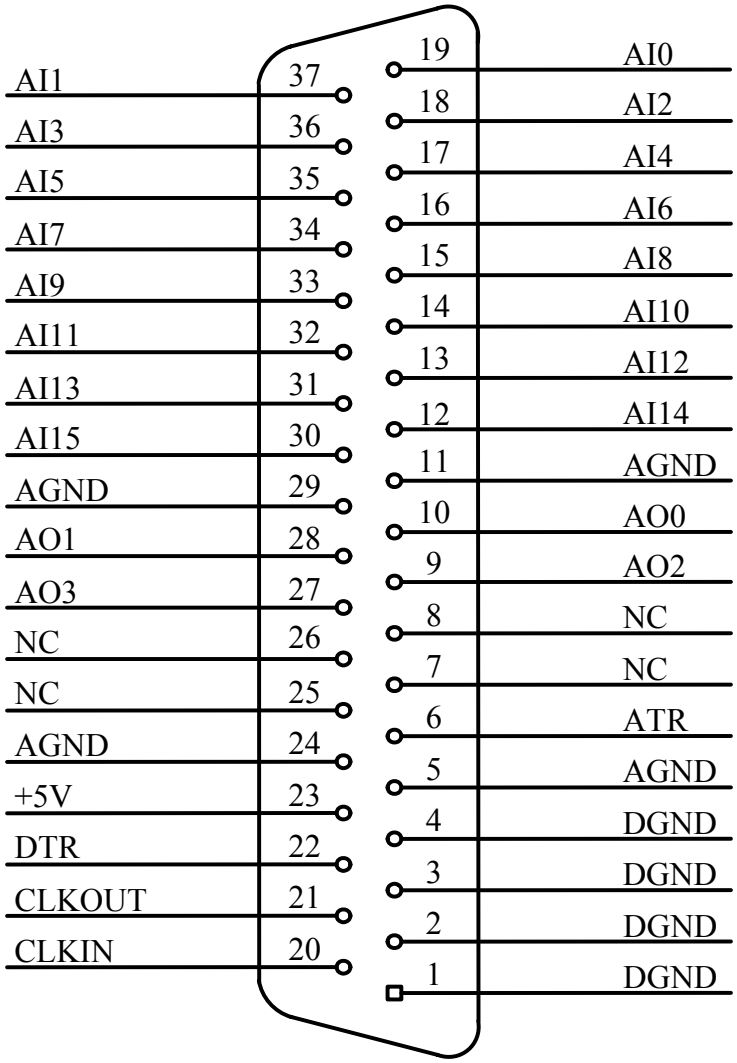
2.2.5 Indicator Status

LED3.3V: 3.3V power indicator, on for normal.

Chapter 3 Signal Connectors

3.1 The Definition of Analog Signal Input and Output Connectors

CN1: 37-pin D-type definition



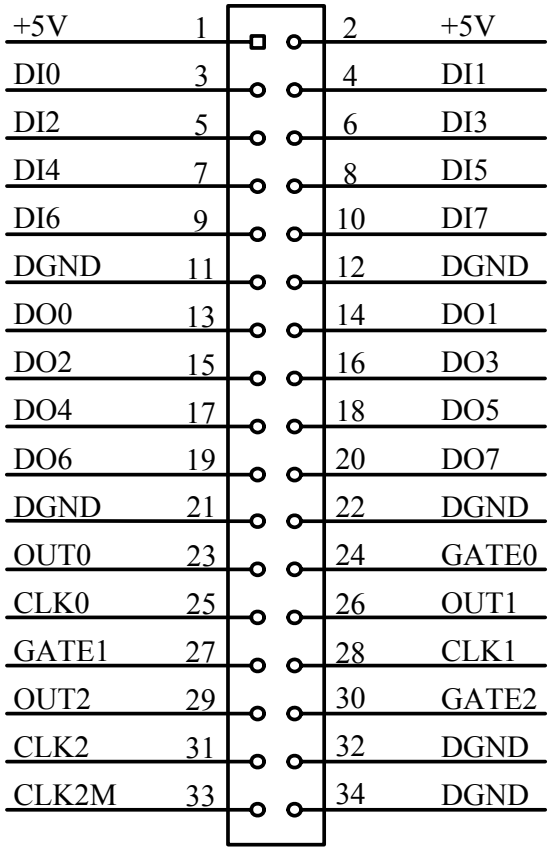
Pin definition about AD:

Pin name	Type	Pin function definition
AI0～AI15	Input	Analog input, reference ground is AGND.
AO0～AO3	Output	Analog output.
AGND		Analog ground. This AGND pin should be connected to the system's AGND plane.
DGND		Digital ground. Ground reference for Digital circuitry. This DGND pin should be connected to the system's DGND plane.
CLKIN	Input	NC.
CLKOUT	Output	NC.

ATR	Input	NC.
DTR	Input	NC.
+5V	Output	Output 5V.
NC		No connection

3.2 The Definition of Digital Signal Input/Output Connectors

P1: 34-pin definition



Pin Name	Feature	Function Definition
DI0~DI7	Input	Digital signal input.
DO0~DO7	Output	Digital signal output.
+5V	Output	Output 5.
CLK2M	Output	On-board 2MHz clock oscillator pulse output, Output cycle 0.5 microseconds, provides the clock source signal for CLK0~CLK2.
CLK0~CLK2	Input	Clock/pulse input pins.
GATE0~GATE2	Input	Gate input pins.
OUT0~OUT2	Output	Output pins.
DGND	GND	Digital ground, when use counter/timer we best choose it as reference ground.

Chapter 4 Connection Ways for Each Signal

4.1 AD Single-ended Input Connection

Single-ended mode can achieve a signal input by one channel, and several signals use the common reference ground. This mode is widely applied in occasions of the small interference and relatively many channels.

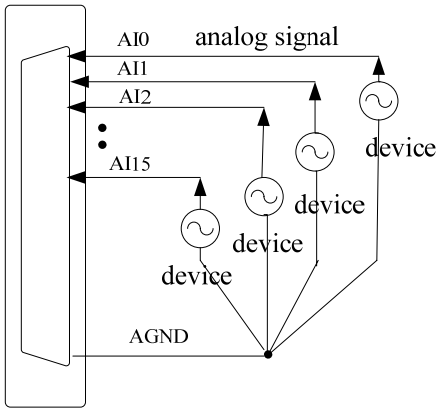


Figure 4.1 single-ended input connection

4.2 AD Double-ended Input Mode

Double-ended input mode, which was also called differential input mode, uses positive and negative channels to input a signal. This mode is mostly used when biggish interference happens and the channel numbers are few. Single-ended/double-ended mode can be set by the software, please refer to USB2816 software manual.

According to the diagram below, USB2833 board can be connected as analog voltage double-ended input mode, which can effectively suppress common-mode interference signal to improve the accuracy of acquisition. Positive side of the 8-channel analog input signal is connected to AI0~AI7, the negative side of the analog input signal is connected to AI8~AI15, equipments in industrial sites share the AGND with USB2833 board.

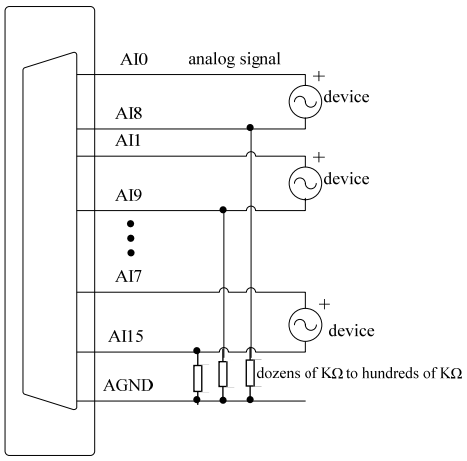


Figure 4.2 double-ended input connection

4.2 Other Connections

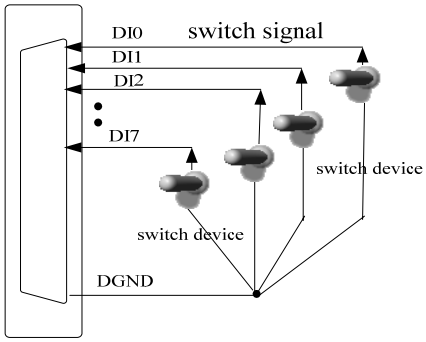


Figure 4.3 digital signal input connection

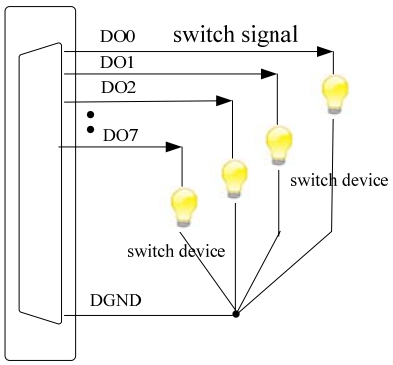


Figure 4.4 digital signal output connection

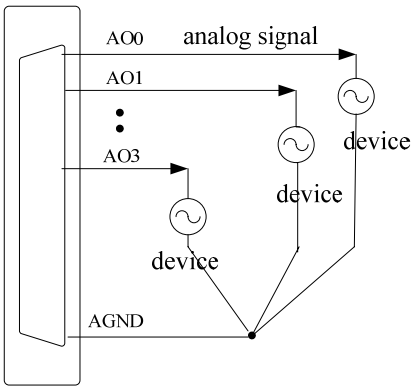


Figure 4.5 Timer/Counter connection

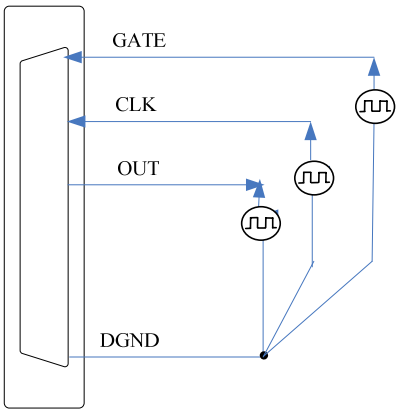
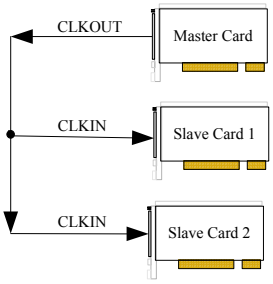


Figure 4.6 Analog signal output connection

4.3 Methods of Realizing the Multi-card Synchronization

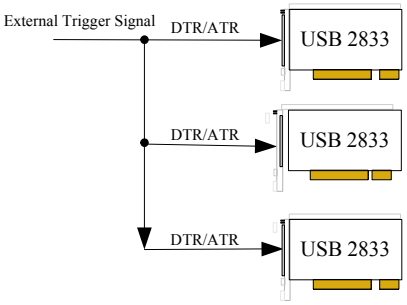
Three methods can realize the synchronization for the USB2833, the first method is using the cascade master-slave card, the second one is using the common external trigger, and the last one is using the common external clock.

When using master-slave cascade card programs, the master card generally uses the internal clock source model, while the slave card uses the external clock source mode. After the master card and the slave card are initialized according to the corresponding clock source mode. At first, start all the slave cards, as the main card has not been activated and there is no output clock signal, so the slave card enters the wait state until the main card was activated. At this moment, the multi-card synchronization has been realized. When you need to sample more than channels of a card, you could consider using the multi-card cascaded model to expand the number of channels.

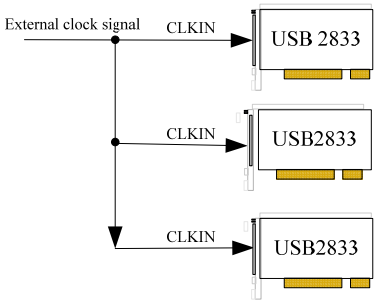


When using the common external trigger, please make sure all parameters of different USB2830 are the same. At first,

configure hardware parameters, and use analog or digital signal triggering (ART,DTR), then connect the signal that will be sampled by USB2833, input triggering signal from DTR pin or ATR, then click “Start Sampling” button, at this time, USB2833 does not sample any signal but waits for external trigger signal. When each module is waiting for external trigger signal, use the common external trigger signal to startup modules, at last, we can realize synchronization data acquisition in this way. See the following figure:



When using the common external clock trigger, please make sure all parameters of different USB2833 are the same. At first, configure hardware parameters, and use external clock, then connect the signal that will be sampled by USB2833, input trigger signal from DTR or ATR pin, then click “Start Sampling” button, at this time, USB2833 does not sample any signal, but wait for external clock signal. When each module is waiting for external clock signal, use the common external clock signal to startup modules, at last, we realize synchronization data acquisition in this way. See the following figure:



Chapter 5 Methods of using Timer/Counter 8254

5.1 The working mode

MODE 0 Interrupt on terminal count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N+1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required)
2) Writing the second byte allows the new count to be loaded on the next CLK pulse

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE=0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulse later, no CLK pulse is needed to load the Counter as this has already been done.

MODE 1 Hardware retriggerable one-shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero.
OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shout is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.
If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

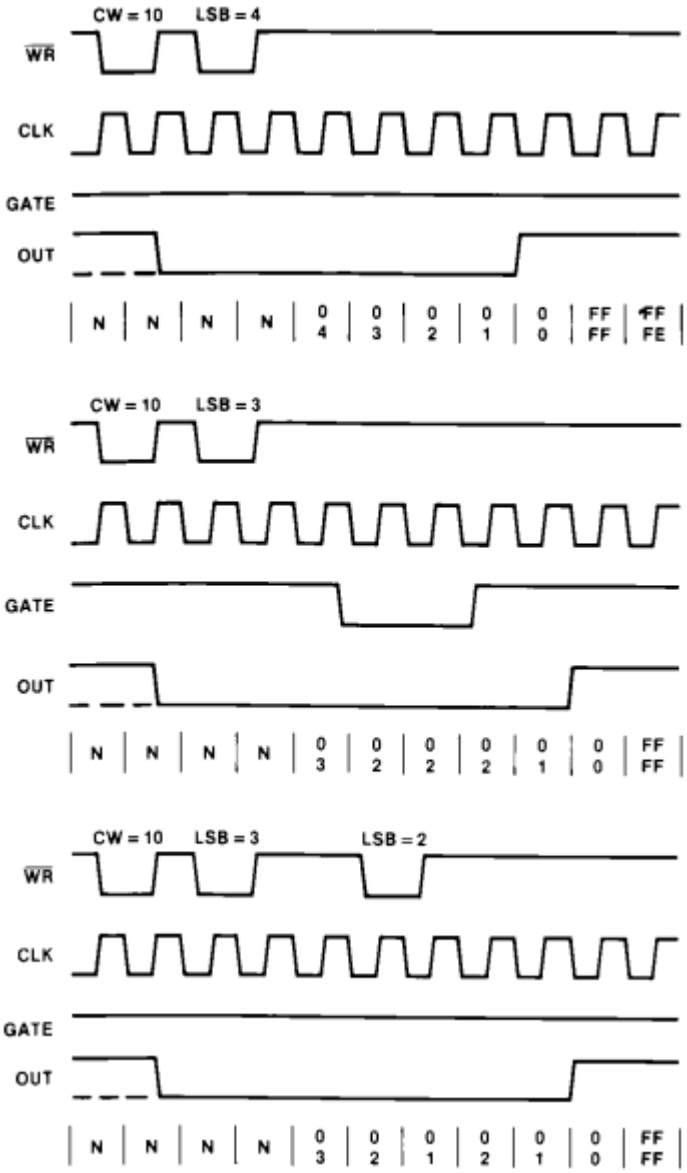


Figure 5.1 Mode 0

NOTE

The following conventions apply to all mode timing diagrams

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.

2. The counter is always selected ($\overline{CS}$ always low)

3. CW stands for "Control Word"; CW=10 means a control word of 10 HEX is written to the counter.

4. LSB stands for "Least Significant Byte" of count.

5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte.

Since the counter is programmed to read/writer LSB only, the most significant byte cannot be read.

N stands for an undefined count.

Vertical lines show transitions between count values.

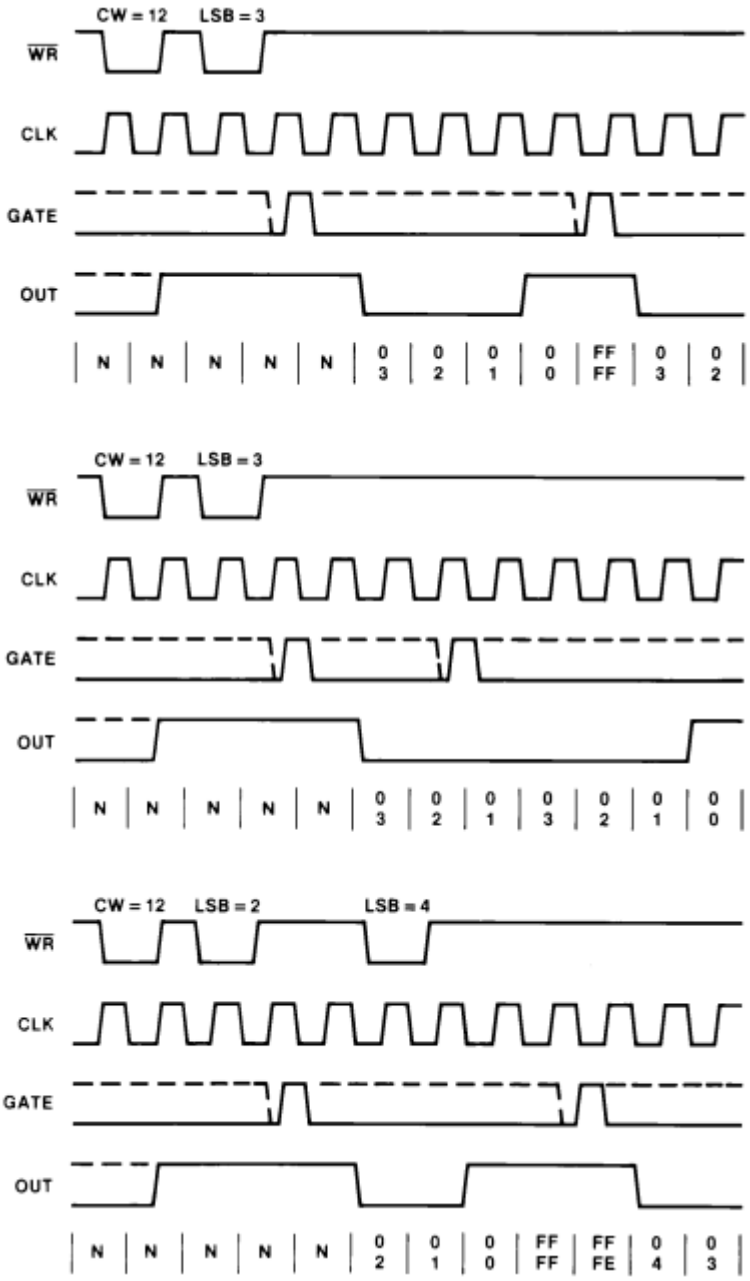


Figure 5.2 Mode 1

MODE 2 Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for on CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode2, a COUNT of 1 I illegal.

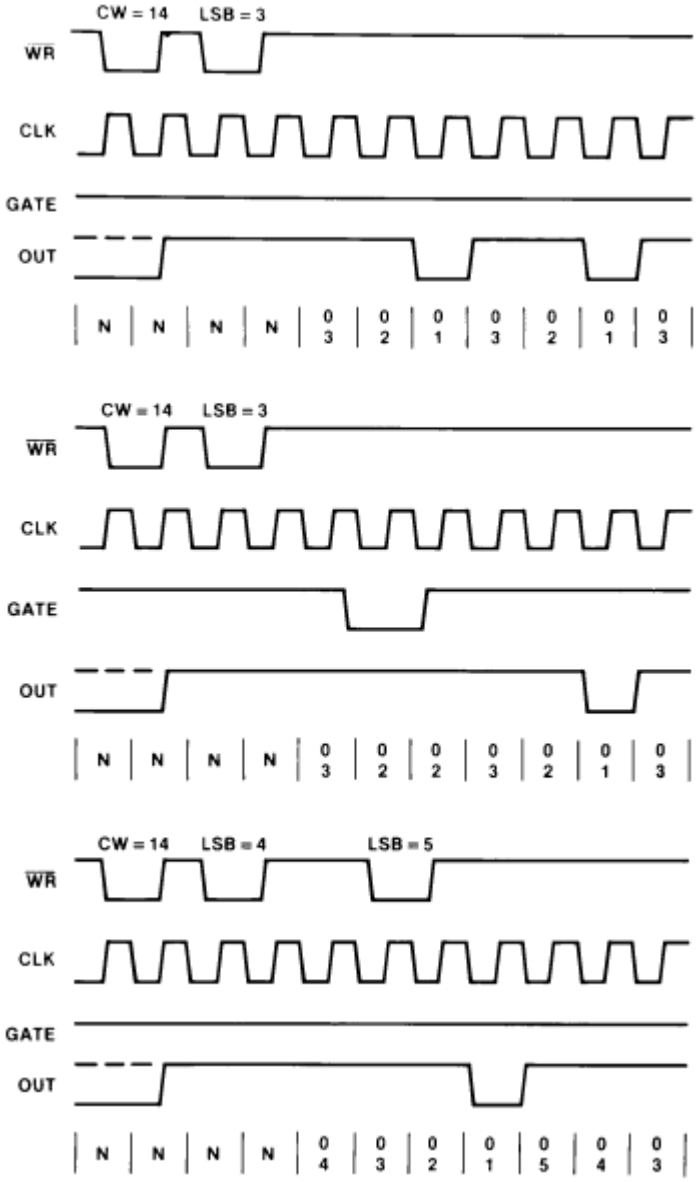


Figure 5.3 Mode 2

Note: A GATE transition should not occur one clock prior to terminal count.

MODE 3 Square wave mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for mainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low while OUT is low, OUT is set high

immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new counter will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires. OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N+1)/2 counts and low for (N-1)/2 counts.

MODE 4 Software triggered strobe
OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is “triggered” by writing the initial count.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after the initial count is written.

If a new count is written during counting, if will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.
This allows the sequence to be ‘‘retriggered’ by software. OUT strobe low N+1 CLK pulses after
the new count of N is written.

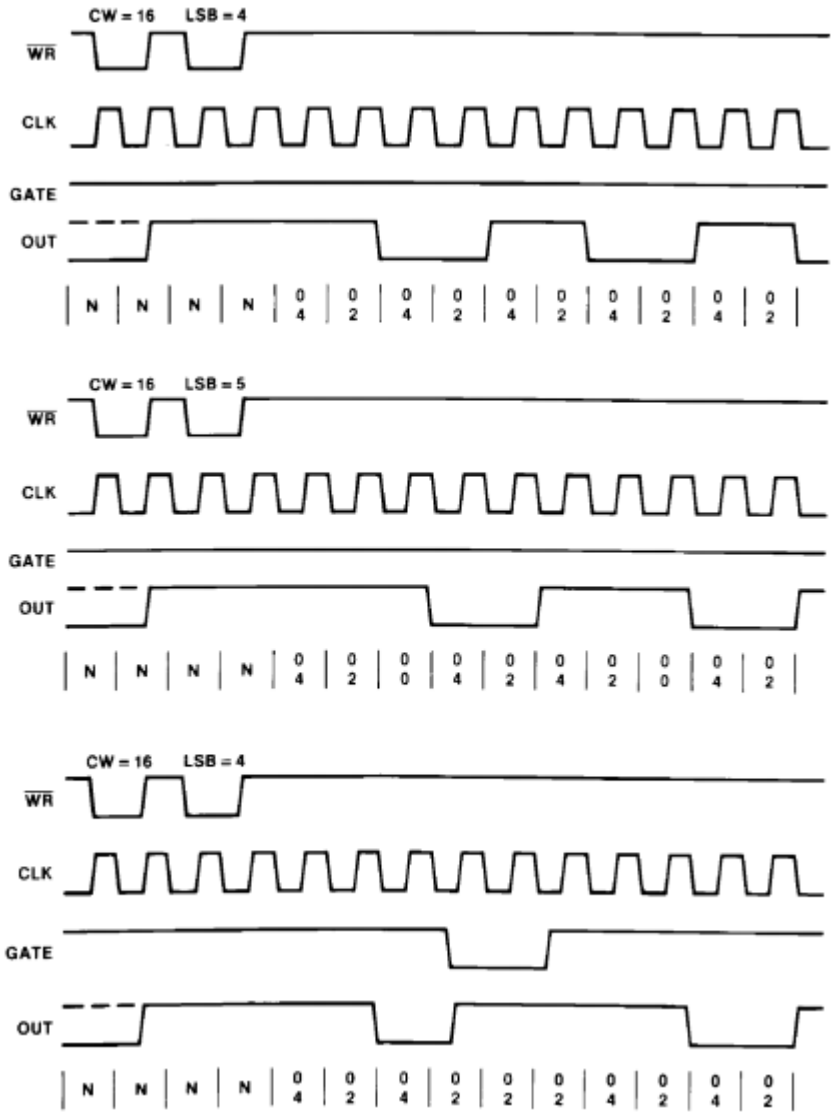


Figure 5.4 Mode 3

Note: A GATE transition should not occur one clock prior to terminal count.

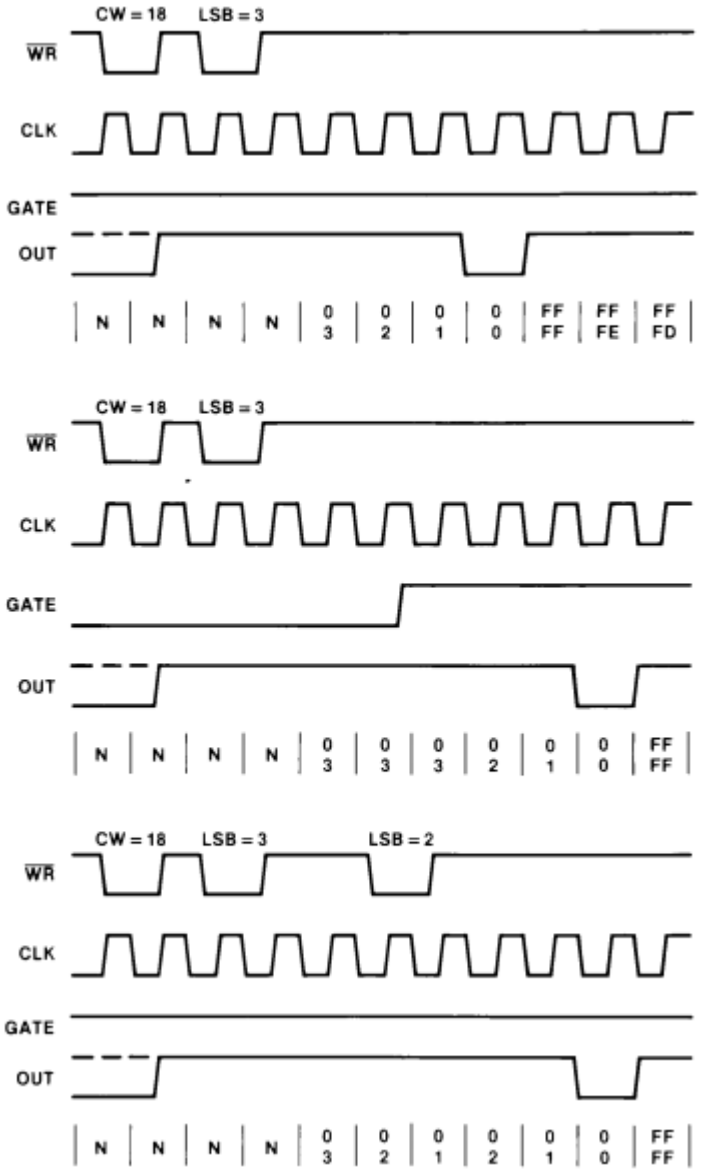


Figure 5.5 Mode 4

MODE 5 Hardware triggered strobe

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+ 1 pulse after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N+1 CLK pulses after any trigger. GATE has no effect on OUT.
If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

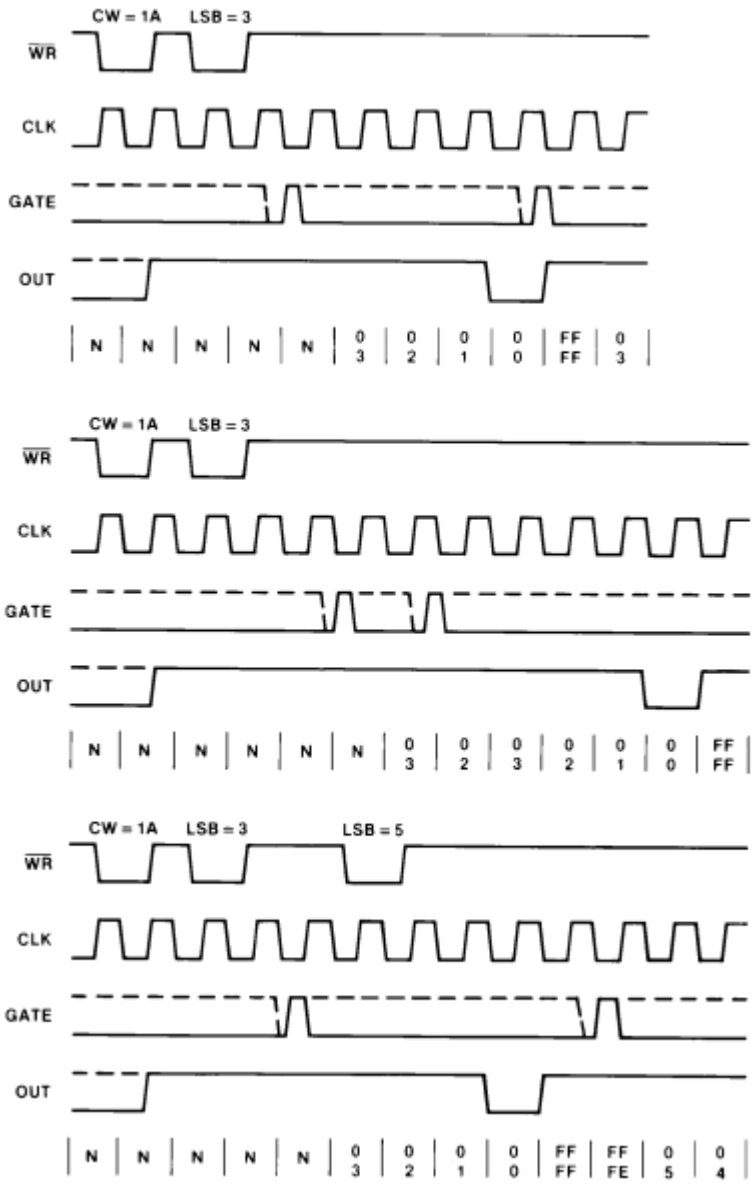
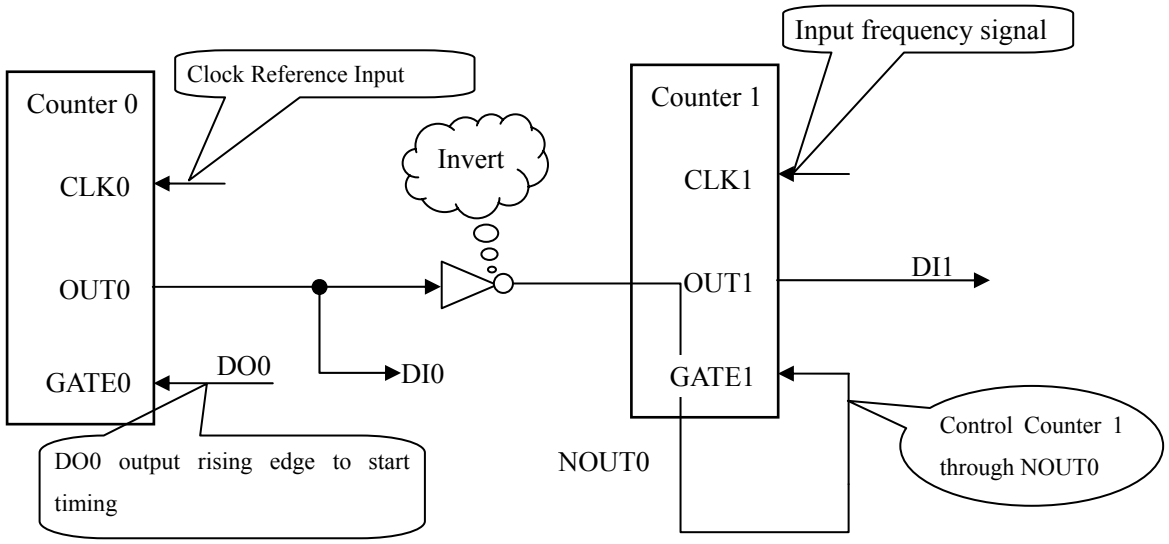


Figure 5.6 Mode 5

5.2 Measure the Frequency of an Unknown Frequency Signal Source.



Note: Counter 0 is timing channel (Mode 1), counter 1 is counting channel (Mode 0, record the number of measured signal pulse). GATE0 is controlled by DO0. Counter 0 is given an initial value which is corresponding to the time in advance. Counter is given the maximum count initial value (FFFFH). When DO0 has a rising edge, counter 0 start to timing count, its "OUT0" becomes low level; "NOUT0" becomes high level. So "GATE1" is high level, counter 1 start to count to record the number of measured signal pulse. If counter1 counting to zero within counter 1' time, "OUT1" turns to high level. Users can read the state of DI1 to judge whether counter 1 is overflow or not. In addition, the user can read DI0 in order to judge whether the frequency measurement has completed. If DIO is high level, the frequency measurement has completed, read the value of counter 1.

At the same time it is necessary to check the state of DI1. If the state of DI1 is low level, the measured frequency is valid. If the state of DI1 is high level, the measured frequency is invalid, and re-measurement is needed. If DO0 has another rising edge, new measure can be re-started.

Chapter 6 Notes, Calibration and Warranty Policy

6.1 Notes

In our products' packing, user can find a user manual, a USB2816 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using USB2833, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of USB2833 module.

6.2 Analog Signal Input Calibration

Every device has to be calibrated before sending from the factory. It is necessary to calibrate the module again if users want to after using for a period of time or changing the input range. In the manual, we introduce how to calibrate USB2833 in ±10V, calibrations of other input ranges are similar.

Prepare a digital voltage instrument which the resolution is more than 5.5 bit, install the USB2833 module, and then power on, warm-up for fifteen minutes.

1) Zero adjustment: select one channel of analog inputs, take the channel AI0for example, connect 0V to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP2 in order to make voltage value is 0.000V or about 0.000V. Zero adjustment of other channels is alike.
2) Full-scale adjustment: select one channel of analog inputs, take the channel AI0 for example, connect 9997.55mV to AI0, and then run ART Data Acquisition Measurement Suite in the WINDOWS. Choose channel 0, ±10V input range and start sampling, adjust potentiometer RP1 in order to make voltage value is 9997.55mV or about 9997.55mV. Full-scale adjustment of other channels is alike.
3) Repeat steps above until meet the requirement.

6.3 Analog Signal Output Calibration

In the manual, we introduce how to calibrate USB2833 in ±5V range; calibrations of other output ranges are similar.

1） Run ART Data Acquisition Measurement Suite in the WINDOWS. Select the DA output test under the menu file operations, select the channel which needs to be calibrated.
2） To set the DA output to 2048, by adjusting the potentiometer RP4 to make AO0 output 0.000V.
3） To set the DA output to 4095, adjust potentiometer RP6 to make AO0 output 4997.55mV.
4） Repeat steps above until meet the requirement.

6.4 DA Use

In demonstration program, the continuous output interval of waveform output can not be carried out; the main objective is to test the strength of DA output.

6.5 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When sending in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.
2. All ART products come with a limited two-year warranty:
   - The warranty period starts on the day the product is shipped from ART's factory
   - For products containing storage devices (hard drives, flash cards, etc.), please back up your data before sending them for repair. ART is not responsible for any loss of data.
   - Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.
3. Our repair service is not covered by ART's guarantee in the following situations:
   - Damage caused by not following instructions in the User's Manual.
   - Damage caused by carelessness on the user's part during product transportation.
   - Damage caused by unsuitable storage environments (i.e. high temperatures, high humidity, or volatile chemicals).
   - Damage from improper repair by unauthorized ART technicians.
   - Products with altered and/or damaged serial numbers are not entitled to our service.
4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.
5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the disc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the USB card. If it is a USB product, it can be directly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system directory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> Corresponding Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponding output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> USB.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.